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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,922	07/08/2004	Jung-Pill Kim	082123-0310458	8429

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,922	KIM, JUNG-PILL	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-16* is/are rejected.

7)☒ Claim(s) *3,10 and 17-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *070804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 08, 2004, claims 1-23 are active in this application.

Information Disclosure Statement

2. The information disclosure statement filed July 08, 2004 has been considered.

Claim Objections

3. Claims 3, 10, 17, 18, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It is unclear as to which "bitline" is being refered to when the phrase "...between a memory cell and the bitline.." was recited in claim 7, line 8. Is it referring to the bitline or the reference bitline?

It appears that claims 19, 21, and their dependents should depend on claim 18 since claim 14 does not support the antecedent bases for their recitations.

Claim Rejections – 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1, 2 and 4-6 are rejected under 35 U.S.C 102(e) as being anticipated by Patel [U.S. Patent #6,839,258].

With respect to claim 1, Patel discloses, in figures 1 and 2, a method of data access, said method comprising: precharging a first bitline [BL11] and a second bitline [BL21]; permitting charge sharing between a capacitance [CA] of a memory cell and the precharged first bitline [BL11]; biasing the precharged second bitline [BL21]; and subsequent to said permitting charge sharing, sensing [via 230] a difference between a potential of the first bitline and a potential of the biased second bitline. See column 3.

With respect to claim 2, Patel discloses, in columns 1-3, that when a particular cell is selected for write or read operations, respective bitlines and wordlines are selected to access that particular cell. By selecting a particular cell, the voltages on the bitlines and wordlines would be altered.

With respect to claim 4, Patel discloses, in column 3, that the sensing of the difference between a potential of the first bitline and a potential of the second bitline is done by the sense amplifier [230]; hence, it is interpreted that the signal outputted from the sense amplifier was amplified.

With respect to claim 5, Patel discloses, in column 3, that the permitting charge sharing is done by way of charging the transistor Q1 thereby includes applying a potential to a gate of a transistor of the memory cell.

With respect to claim 6, Patel discloses, in column 3, that the biasing includes applying a potential to charge capacitor CA coupled to the bitline.

6. Claims 7-9 are rejected under 35 U.S.C 102(e) as being anticipated by Patel [U.S. Patent #6,839,258].

With respect to claim 7, Patel discloses, in figures 1 and 2, a method of data access, said method comprising: selecting a wordline [charged WL13]; asserting a bias signal corresponding to the wordline [by selecting a particular cell, the voltages on the wordlines and bitlines would be altered]; and sensing a difference between a potential of a bitline [active bitline – see column 3] coupled to the wordline and a potential of a reference bitline [dynamic storage node – see column 3], wherein charge sharing between a memory cell and the bitline occurs as a consequence of said selecting a wordline, and wherein the potential of the reference bitline is altered as a consequence of said asserting a bias signal. See column 3.

With respect to claim 8, Patel discloses, in column 3, that a charge given to transistor Q1 during the accessing operation was made; however, it is known that before access is being made to a given cell, a particular cell needs to be selected via its wordline and bitline.

With respect to claim 9, Patel discloses, in columns 1-3, that when a particular cell is selected for write or read operations, respective bitlines and wordlines are selected to access that particular cell. By selecting a particular cell, the voltages on the bitlines and wordlines would be altered.

7. Claims 11-13 are rejected under 35 U.S.C 102(e) as being anticipated by Patel [U.S. Patent #6,839,258].

With respect to claim 11, Patel discloses, in figures 1 and 2, a method of data access, said method comprising: precharging a first bitline [BL11] and a second bitline [BL21]; permitting charge sharing between a capacitance [CA] of a memory cell and the precharged first bitline [BL11]; biasing a selected one of the precharged bitlines [BL21]; and subsequent to said permitting charge sharing and said biasing, sensing [via 230] a difference between a potential of the first bitline and a potential of the second bitline. See column 3.

With respect to claim 12, Patel discloses, in columns 1-3, that when a particular cell is selected for write or read operations, respective bitlines and wordlines are selected to access that particular cell. By selecting a particular cell, the voltages on the bitlines and wordlines would be altered.

With respect to claim 13, Patel discloses, in column 3, that the biasing includes applying a potential to charge capacitor CA coupled to the bitline.

8. Claims 14-16 are rejected under 35 U.S.C 102(e) as being anticipated by

Tanaka et al. [U.S. Patent #5,559,737].

With respect to claim 14, Tanaka et al. disclose, in figure 5, a storage device comprising: a precharging circuit [91] configured and arranged to precharge a bitline [2] and a reference bitline [12]; a memory cell [1] configured and arranged to share charge with the bitline [memory devices convey data to and from memory cells by way of the bitlines]; a bias circuit [6 and 16] configured and arranged to alter a potential of the reference bitline; and a sense amplifier [20] configured and arranged to sense a difference between a potential of the bitline and a potential of the reference bitline.

With respect to claim 15, Tanaka et al. disclose, in figure 5, that the memory cell includes a transistor [1]. Tanaka et al. also state that there exists capacitance within the memory array – see column 9.

With respect to claim 16, Tanaka et al. disclose, in figure 5, the memory cell is coupled to a wordline [electrode connecting to the gate of memory cell 1] and is further configured and arranged to share charge with the bitline upon a predetermined alteration in a potential of the wordline. It is noted that when a particular cell is selected for write or read operations, respective bitlines and wordlines are selected to access that particular cell. By selecting a particular cell, the voltages on the bitlines and wordlines would be altered.

Allowable Subject Matter

9. The following is an Examiner's statement of reasons for the indication of

allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Biasing includes reducing a potential of the second bitline.
- The potential of the reference bitline is reduced as a consequence of said asserting a bias signal.
- The bias circuit is configured and arranged to reduce a potential of the reference bitline.
- The bias circuit includes a bias capacitor coupled to the reference bitline.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
June 8, 2005

MICHAEL T[illegible]
PRIMARY EX[illegible]